REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Office Action of November 15, 2004 has been received and its contents carefully reviewed.

Claims 1-24 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

Applicants appreciate the indication of allowable subject matter in claim 23.

In the Office Action, the Examiner rejected claims 1-20 and 24 under 35 U.S.C. § 103(a) as being unpatentable over the related art illustrated in Figures 1-6 in view of Kang (U.S. Patent No. 6,621,547). This rejection is respectfully traversed and reconsideration is requested.

Specifically, the present application claims the benefit of priority under 35 U.S.C. § 119(a)-(d) to Korean Patent Application No. 2000-29725, filed on May 31, 2000. Kang has an effective reference date of December 15, 2000. Accordingly, Applicants submit that the present foreign priority filing date antedates the effective reference date of Kang and hereby submit an English language translation of Korean Patent Application No. 2000-29725, perfecting the present claim to foreign priority (a certified copy of Korean Patent Application No. 2000-29725 was filed on August 20, 2001). Consequently, Applicants respectfully submit that Kang is not available as prior art and request withdrawal of the present rejection under 35 U.S.C. § 103(a).

In the Office Action, the Examiner rejected claims 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over the related art illustrated in Figures 1-6 in view of Kang and further in view of Ito et al. (U.S. Patent No. 5,748,179). This rejection is respectfully traversed and reconsideration is requested.

Claims 21 and 22 depend variously from claims 1 and 20, which as discussed above, are patentable over the related art illustrated in Figures 1-6 in view of Kang. Therefore, Applicants respectfully submit that claims 21 and 22, are patentable over the related art illustrated in Figures 1-6 in view of Kang and further in view of Ito et al. by virtue of their various dependence from claims 1 and 20.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: February 15, 2005

Respectfully submitted,

By [signature] Reg. No 41786

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VERIFICATION OF TRANSLATION

I, Eun-Jung Han of 901 Seoyoung Bldg., 158-12, Samsung-dong, Kangnam-ku, Seoul, 135-090, Korea, declare that I have a thorough knowledge of the Korean and English languages, and the writings contained in the following pages are correct English translation of the specification and claims of Korean Patent Application No. 2000-29725.

This 15th day of February, 2005

By:

[Eun-Jung Han]

KOREAN INTELLECTUAL

PROPERTY OFFICE

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

Application Number : **PATENT-2000-29725**

Date of Application : **May 31, 2000**

Applicant(s) : **LG. PHILIPS LCD CO., LTD.**

April 23, 2001

COMMISSIONER

[BIBLIOGRAPHICAL DOCUMENTS]

[TITLE OF DOCUMENT] PATENT APPLICATION

[CLASSIFICATION] PATENT

[RECIPIENT] COMMISSIONER

[SUBMISSION DATE] 2000. 05. 31

[TITLE OF INVENTION IN KOREAN] 액정표시장치 제조방법

[TITLE OF INVENTION IN ENGLISH] method for fabricating liquid crystal display device

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[APPLICANT CORD] 1-1998-101865-5

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[NAME] Jung, Won-Ki

[ATTORNEY CORD] 9-1998-000534-2

[ALL-INCLUSIVE AUTHORIZATION REGISTRATION NUMBER] 1999-001832-7

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[NATIONALITY] KR

[REQUEST FOR EXAMINATION] **YES**

[PURPORT] We submit application as above under the article 42 of the Patent Law and request examination as above under the article 60 of the Patent Law.

Attorney Jung, Won-Ki (seal)

[FEES]

[BASIC APPLICATION FEE]	20 pages	29,000	won
[ADDITIONAL APPLICATION FEE]	2 pages	2,000	won
[PRIORITY FEE]	0 things	0	won
[EXAMINATION REQUEST FEE]	3 clamis	205,000	Won

[TOTAL] 236,000 Won

[ENCLOSED] 1. Abstract, Specifications (with Drawings) - 1 set

[DOCUMENT OF ABSTRACT]

[ABSTRACT]

The present invention relates to a liquid crystal display (LCD) device, and in a liquid crystal display device including a gate drive IC and a source drive IC disposed one sides of gate lines and data lines crossing each other and a gate PCB and a source PCB connected to the gate drive IC and the source drive IC, respectively, an additional FPC is not attached as a means for transmitting gate signals of V_{com}, V_{gh}, V_{gl}, V_{cc}, G_{sp}, G_{sc}, G_{oe}, and Gnd to the gate PCB via the source PCB, and gate transmitting lines are directly formed on a lower substrate (array substrate) of a liquid crystal panel, wherein the gate transmitting line transmitting the V_{gl} signal among the gate transmitting lines has a resistance of below maximum 30 Ω.

In the above structure, since additional FPC is not used, manufacturing costs are lowered, and a liquid crystal display device having no cross-talk may be fabricated because there is no distortion of the V_{gl} signal waveform applied to the gate line.

[REPRESENTATIVE FIGURE]

FIG. 7

[SPECIFICATIONS]

[NAME OF INVENTION]

Method for fabricating liquid crystal display device

[BRIEF EXPLANATION OF FIGURES]

FIG. 1 is a cross-sectional view illustrating a structure of a tape carrier package (TCP),

FIG. 2 is a plan view schematically illustrating a liquid crystal display (LCD) device according to the related art,

FIG. 3 is a plan view schematically illustrating an LCD device having a structure of improved gate transmitting lines according to the related art,

FIG. 4 is an expanded view of a portion "A" of Figure 3,

FIG. 5 is a plan view illustrating a window pattern on an LC panel used for a cross-talk test,

FIG. 6A and 6B are views illustrating waveforms in border portions around a window region of the LC panel when the window pattern of Figure 5 is displayed,

FIG. 7 is an expanded plan view illustrating a part of an array substrate for an LCD device according to the present invention, and

FIG. 8 is a view illustrating waveforms of a V_{gl} signal in a window region, a peripheral region and a border portion therebetween displayed on an LC panel according to the present invention.

* Explanation of major parts in the figures *

135: gate transmitting lines	135a: Vgl gate transmitting line
141: gate lines	143: date lines

145: gate drive IC

147: source drive IC

149: gate PCB

150: liquid crystal display device

151: source PCB

153: liquid crystal panel

161: gate pad

163: source pad

[DETAILED DESCRIPTION OF INVENTION]

[OBJECT OF INVENTION]

[TECHNICAL FIELD OF THE INVENTION AND PRIOR ART OF THE FIELD]

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to gate transmitting lines, which serve as terminal lines that interconnect a source printed circuit board (hereinafter referred to as "source PCB") and a gate printed circuit board (hereinafter referred to as "gate PCB") connected to a liquid crystal panel of the LCD device to thereby transmit signals.

Generally, a liquid crystal display (LCD) device includes a transparent upper substrate, a transparent lower substrate, and liquid crystal (LC) interposed therebetween.

In an active matrix LCD (AM LCD) device, a plurality of switching elements corresponding to a plurality of pixels are formed in a matrix shape on the lower substrate.

For example, a thin film transistor including a source electrode, a drain electrode, and a gate electrode may be used as the switching element, and at this time, a gate line that provides a scanning signal to the gate electrode and a data line that provides a data signal to the source electrode are formed, wherein the gate line and the data line cross with each other and an insulating layer is formed between the gate and data lines.

In addition, a pixel electrode contacting the drain electrode is formed on each pixel.

Meanwhile, on the upper substrate, a common electrode is formed by depositing a transparent conductive material.

At this time, in case of a color LCD device, a color filter is formed on the upper substrate, and then the common electrode is formed on the color filter.

The above-mentioned lower substrate and the upper substrate are attached to each other using a sealant therebetween, and then a liquid crystal is interposed between the upper and lower substrates such that a liquid crystal panel is produced.

In the above-mentioned LCD device, the scanning signal applied to the gate electrode is properly controlled such that an electric signal is applied to the liquid crystal via the data line, and since the variable data signal gradually changes the polarization state of the liquid crystal, various gray levels are displayed in the LCD device.

The LCD device is equipped with a drive IC (Integrated Circuit), which serves to apply electric signals to each electric line formed on the lower substrate of the LC panel, in various methods, and this technology may be variously adopted.

For example, there are methods such as chip on board (COB), chip on glass (COG), and tape carrier package (TCP) methods.

The COB (chip on board) method is adopted for a segment type LCD device or a panel having a low resolution, and since a small number of leads are used, the drive IC is installed on a printed circuit board (PCB), whereby the leads of the PCB are connected with the LC panel via a proper method.

However, as the LCD devices become to have a high resolution, it is difficult to install the drive IC having a great number of leads on the above-mentioned PCB.

In another method, the COG method, since chips are directly installed on the panel, the connection stability is good, and a minute pitch is applicable for the installation because of no additional pads.

In the COG method, a multi-layered flexible printed circuit board (hereinafter referred to as "FPC") instead of the PCB is connected to the panel via an anisotropic conductive film (ACF), and thus input signals are transmitted to the drive IC.

The above-mentioned COG method has advantages of low cost and high stability.

On the other hand, in the COG method, it is difficult to repair against troubles, and the panel should be enlarged because a pad portion is further needed to install the IC by the COG method.

In another method, the tape carrier package (hereinafter referred to as "TCP") method, the drive IC chip is installed on a polymer film.

The TCP method is widely used for the LCD device as well as products that need small, thin, and light packages such as mobile phones.

FIG. 1 is a cross-sectional view illustrating a structure of a conventional liquid crystal display device to which a tape carrier package (TCP) is installed

As shown, in the structure of the tape carrier package Z, a drive IC 17 is installed on a polymer film 19, and the polymer film, on which the drive IC chip is installed, is connected with a lower substrate of a liquid crystal panel, which includes an upper substrate 13 and the lower substrate 11 attached with each other, and a printed circuit board 20 using an anisotropic conductive film (ACF) 18.

The above-mentioned TCP applies signals to both ends or just one end of a data line (not shown) and both ends or just one end of a gate line (not shown) of an array substrate to

thereby drive the panel. (In the specifications, the above-mentioned TCP method may be explained as an example of the method for installing the drive IC.)

FIG. 2 is a plan view schematically illustrating a liquid crystal display (LCD) device on which a drive IC is installed by using the TCP method.

As shown, the LCD device 24 includes a lower substrate 23 on which a gate line 22 and a data line 28 are formed to cross with each other, an upper substrate 25 attached with the lower substrate 23 to constitute a liquid crystal panel, a source TCP 27 which is disposed at one side of the date line 28 and on which a source drive IC chip connected to the data line 28 and applying signals to the data line 28 is installed, and a gate TCP 29 which is disposed at one side of the gate line 22 and on which a gate drive IC chip connected the gate line 22 and providing scanning signals to the gate line is installed.

In addition, the LCD device includes a source PCB 31 that is connected to the source TCP 27 and functions as an intermediation means for transmitting exterior control signals and a gate PCB 33 that is connected to the gate TCP 29.

At this time, the exterior circuit for controlling the gate drive IC flows into the gate PCB 33 through the source PCB 31, and at the same time, the gate signals flowing in the source PCB 31 are provided to the gate PCB 33 using the above-mentioned FPC.

That is to say, the gate signals including V_{com}, V_{gh}, V_{gl}, V_{cc}, G_{sp}, G_{sc}, G_{oe}, and G_{nd} for driving the gate TCP are provided to the gate PCB from the source PCB through the FPC 35.

Among the signals, a gate high voltage V_{gh} and a gate low voltage V_{gl} directly pass through the gate line, a common voltage V_{com} is applied to the upper substrate of the LC panel, G_{sc} and G_{oe} serve to control the gate signals passing through the gate line, and G_{sp} serves to control the drive IC.

At this time, in the above-mentioned structure, since the gate control signals are transmitted using the additional FPC 35, material costs for fabricating the LCD device may increase, and inferiority in the LC module may occur due to a soldering error when the FPC 35 is connected to the gate PCB and the source PCB.

Therefore, to solve the above-mentioned problem, recently, instead of the FPC, lines transmitting the gate signals have been directly patterned on the lower substrate of the LC panel.

FIG. 3 shows an improved structure as compared with the related and a plan view of a part of an LCD device including gate transmitting lines formed on a substrate.

As shown, gate transmitting lines 45 are formed on a lower substrate 23 to transmit signals from the source PCB 31 to the gate PCB 33.

This conductive metal includes aluminum (Al), molybdenum (Mo), chromium (Cr), alloys thereof, and the like.

FIG. 4 is an expanded view of the gate transmitting lines in a portion "A" of Figure 3.

As shown, the number of the gate transmitting lines 45 formed on the lower substrate 23 of Figure 3 is at least eight, and at this time, signals through the gate transmitting lines 45 include V_{com}, V_{gh}, V_{gl}, V_{cc}, G_{sp}, G_{sc}, G_{oe}, and G_{nd}, respectively.

Each gate transmitting line 45 is disposed between a source pad 47 and a gate pad 49, and dummy pads are preferably further formed between first to eighth transmitting lines.

An array substrate for an LCD paned fabricated according as mentioned above takes a test for a display quality, and the typical example is to measure cross-talk.

Generally, in a line addressing method, the cross-talk distorting signals is generated according to information of a pixel adjacent thereto, and with reference to Figure 5, a method to measure the cross-talk is explained.

FIG. 5 is a plan view illustrating a window displayed on an LC panel for a cross-talk test.

As shown, a window 63 is displayed on a center of a display area 61, and a window area and peripheral gray portions are driven to have different gray scales. Thus, the degree of the cross-talk is shown by normalizing difference of brightness in the peripheral gray portions. (At this time, the window shows a black state, and the upper/lower portions of the window show a grey state.)

That is to say, it is most sensitive to measure the cross-talk such that the middle window 63 is driven to be darkest and large voltage having sharp slope of an electro-optic transmitting curve is applied to the peripheral portions.

As shown, an only middle gray level is shown in the window during t1 and t3 of 1 frame, and both a black level and a middle gray level are shown during a t2 time.

At this time, the middle gray level of the t2 time differs from the middle gray level of the t1 or t3 time to right and left sides of the black window area 63.

The abnormal display state shown like this is referred to as horizontal cross-talk.

That is, the horizontal cross-talk is a phenomenon that is shown like a dim shadow because brightness of the left and right portions of the pattern is affected when a black window area is displayed on the LC panel.

The above-mentioned cross-talk is caused by the following various reasons:

First, a distortion of a common signal due to a signal coupling between a data signal and the common signal;

Second, a distortion of signals due to a sheet resistance of the pixel electrode or a contact resistance of the pad portions;

Third, a current driving capacity of the source drive IC and the data drive IC; and

Fourth, a low capacitance of the thin film transistor.

There are various reasons, and especially, the main reason causing the horizontal cross-talk shown in specific models of LC panels is a remarkable distortion of the gate low voltage V_{gl} signal among the 8 signals in a structure that the gate transmitting lines are directly patterned on the substrate.

Since the V_{gl} voltage waveform is simultaneously applied to all the gate lines, large currents are consumed, and thus the gate transmitting line formed on the substrate has not sufficient width and length for the V_{gl} signals to pass therethrough without some distortion.

Therefore, the V_{gl} signal waveform is heavily distorted due to the resistance of the gate transmitting lines, and the distortion of the V_{gl} waveform affects a waveform of a data signal, whereby a voltage applied to the liquid crystal, which is determined by difference between the data voltage and the common voltage, is changed in result and thus differs from a voltage applied to the liquid crystal when there is no the window pattern.

The voltage difference causes a visible horizontal cross-talk on the LC panel.

FIGs. 6A and 6B are views illustrating waveforms in border portions around a window region of the LC panel when the window pattern of Figure 5 is displayed.(Explanation will be made with reference to Figure 3 and Figure 5.)

Figure 6A shows waveforms of the V_{gl} signals that are measured in a window region 63 of Figure 5 and upper and lower boundaries of the window region in a first case to directly apply voltage output from the source PCB 31 of Figure 3 not through the gate transmitting lines 45 of Figure 3, and Figure 6B shows waveforms of the V_{gl} signals that are measured in the boundaries of the window region in a second case to apply voltage to the gate PCB 33 through the source PCB 31 and the gate transmitting lines 45.(At this time, the waveforms are measured along a vertical direction of the display across the window region.)

As shown in Figure 6A, in the first case, there is a small difference of about 4.2 mV between the waveform measured in peripheral portions around the boundaries and the V_{gl} signals 65a or 65b measured in the window region 63 of Figure 5 and the boundaries 64, and as shown in Figure 6B, in the second case, there is a large voltage difference of about 67 mV between the V_{gl} signal measured in the peripheral portions and the V_{gl} signals 65a and 65b measured in the boundaries 64 of Figure 5 of the window regions 63 of Figure 5.

Accordingly, it is possible to come to a conclusion that the distortion of the V_{gl} signal 65 is largely affected by the resistance of the gate transmitting lines connected to the source pad and the gate pad.

[TECHNICAL SUBJECT OF INVENTION]

Accordingly, the present invention has an object to provide an LCD device manufactured through a low cost efficiency without poor lines by using a new line connecting method instead of the FPC.

[CONSTRUCTION AND OPERATION OF INVENTION]

To achieve the above-mentioned object, a liquid crystal display device of the present invention includes a liquid crystal panel having an upper substrate and a lower substrate, which is attached to the upper substrate with a sealant and includes a plurality of source pads and a plurality of gate pads; a source PCB transmitting signals to the plurality of source pads; and a plurality of gate transmitting lines connecting the plurality of gate pads with the plurality of source pads adjacent to a corner of the lower substrate so as to transmit gate signals (V_{com}, V_{gh}, V_{gl}, V_{cc}, G_{sp}, G_{sc}, G_{oe}, and Gnd) from an exterior circuit to a gate PCB

through the source PCB, wherein the conductive line transmitting the V_{gl} signal has a resistance of below 30 Ω.

The gate transmitting lines are at least eight.

The device further comprises dummy pads between the plurality of source pads and between the plurality of gate pads.

Hereinafter, an exemplary embodiment of the present invention will be explained with reference to attached drawings.

-- embodiment --

In the embodiment of the present invention, additional FPC parts are not used, and a liquid crystal display device is manufactured by directly forming gate transmitting lines corresponding to the FPC on a substrate and by controlling resistance of the gate transmitting line for a V_{gl} signal so that the V_{gl} signal waveform among the gate signals is not distorted.

FIG. 7 is an expanded plan view illustrating a part of an array substrate for an LCD device according to the present invention

In the present invention, to prevent horizontal cross-talk of the display due to the distortion of the V_{gl} signal waveform, the resistance of the V_{gl} signal line 135a among the eight gate transmitting lines 135 is lowered to thereby reduce the distortion of the V_{gl} signal waveform.

Various methods may be adopted to reduce the resistance, for example, using a material of low resistivity as a conductive line for the gate transmitting line 135, shorting a length of the line, or widening a width of the line if the line has a fixed length.

As shown, the LCD device 150 includes a liquid crystal panel 153, which has gate lines 141, data lines 143, thin film transistors T and pixels, a gate drive IC 145, which applies scanning signals to the gate lines 141 of the liquid crystal panel 153, a source drive IC 147,

which applies data signals to the data lines 143, a gate PCB 149, which applies a signal to the gate drive IC 145, and a source PCB 151, which applies a signal to the source drive IC 147.

At this time, on a corner of the liquid crystal panel 153, gate transmitting lines 135 are formed and are used for applying the gate signals including V_{com}, V_{gh}, V_{gl}, V_{cc}, G_{sp}, G_{sc}, G_{oe}, and G_{nd} to the gate PCB 149.

It is desirable to form dummy pads between first to eighth gate transmitting lines 135.

This is why there can be electrical problems due to voltage difference between the lines if the lines having the different voltages may be adjacent to each other because respective lines have different voltages.

The gate transmitting lines 135 are formed along the corner of the liquid crystal panel 153 and are connected to both gate pads 161 and data pads 163 adjacent to the corner of the liquid crystal panel 153.

At this time, the gate transmitting lines 135 have different lengths depending on their position, and the lines have a resistance of 100 Ω. Especially, the gate transmitting line 135a transmitting the V_{gl} among the eight signals has a resistance lower than 30 Ω.

As stated above, by lowering the resistance of the gate transmitting line 135, the waveform distortion of the gate signal V_{gl} due to the relatively high resistance is prevented, and when the resistance is below 30 Ω, cross-talk of the LC panel is invisible to users.

In the present invention, to achieve the above-mentioned resistance, an area of the gate line transmitting the V_{gl} signal increases.

Various methods may be applied to achieve the V_{gl} gate transmitting line having the resistance lower than 30 Ω.

FIG. 8 is a view illustrating waveforms laying stress on a window pattern for testing a liquid crystal panel manufactured according to the present invention. (The explanation will be made with respect to Figure 5)

The waveforms are measured in boundaries of the window region when the resistance of the V_{gl} signal transmitting line 135a of Figure 7 among the resistances of the gate line below 30 Ω is 20 Ω.

The illustrated view is a picture of a real measuring apparatus, and the view shows a very low V_{gl} voltage difference of 25 mV as compared with the voltage difference shown in Figure 6B.

[EFFECT OF INVENTION]

Accordingly, the resistance is lowered by increasing the area of the gate transmitting line transmitting the V_{gl} signal to thereby minimize the distortion of the V_{gl} signal waveform, and thus the cross-talk in the liquid crystal panel due to the signal distortion can be prevented.

Therefore, a liquid crystal display device having no poor image quality is manufactured.

[RANGE OF CLAIMS]

[CLAIM 1]

A liquid crystal display device, comprising:

a liquid crystal panel having an upper substrate and a lower substrate, which is attached to the upper substrate with a sealant and includes a plurality of source pads and a plurality of gate pads;

a source PCB transmitting signals to the plurality of source pads; and

a plurality of gate transmitting lines connecting the plurality of gate pads with the plurality of source pads adjacent to a corner of the lower substrate so as to transmit gate signals (V_{com}, V_{gh}, V_{gl}, V_{cc}, G_{sp}, G_{sc}, G_{oe}, and Gnd) from an exterior circuit to a gate PCB through the source PCB, wherein the conductive line transmitting the V_{gl} signal has a resistance of below 30 Ω.

[CLAIM 2]

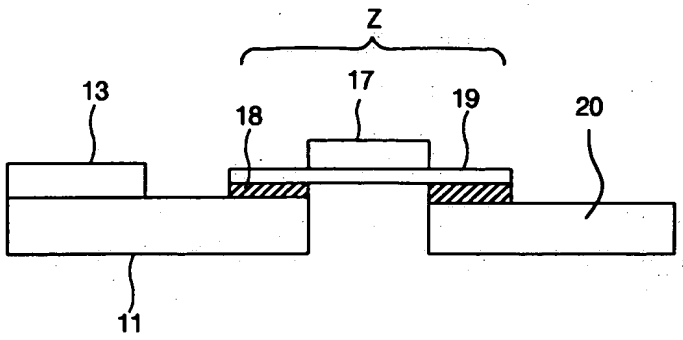
The device according to claim 1, wherein the gate transmitting lines are at least eight.

[CLAIM 3]

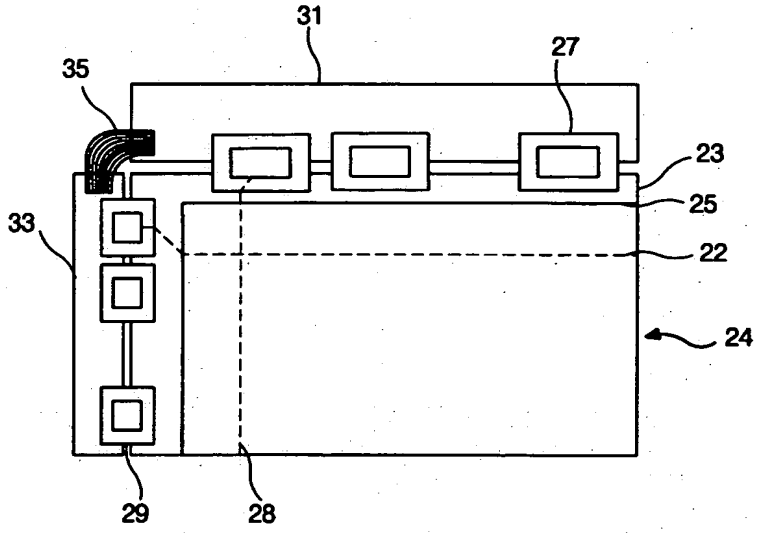
The device according to claim 1, further comprising dummy pads between the plurality of source pads and between the plurality of gate pads.

[DRAWINGS]

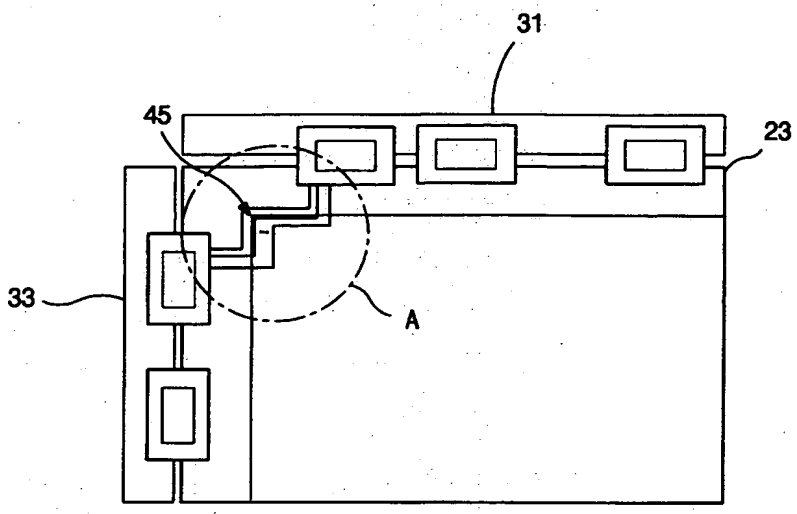
[Fig. 1]



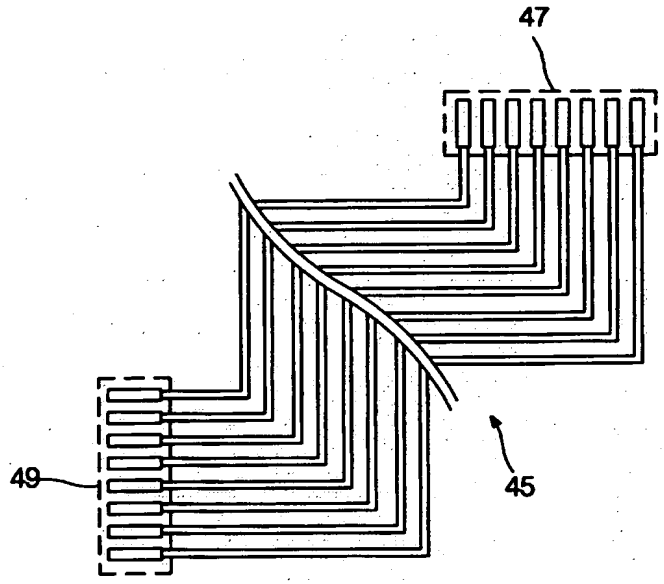
[Fig. 2]



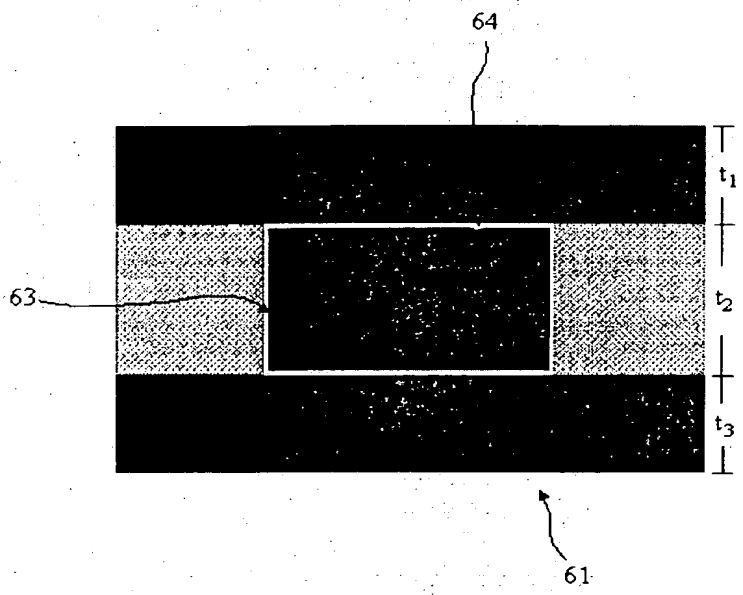
[Fig. 3]



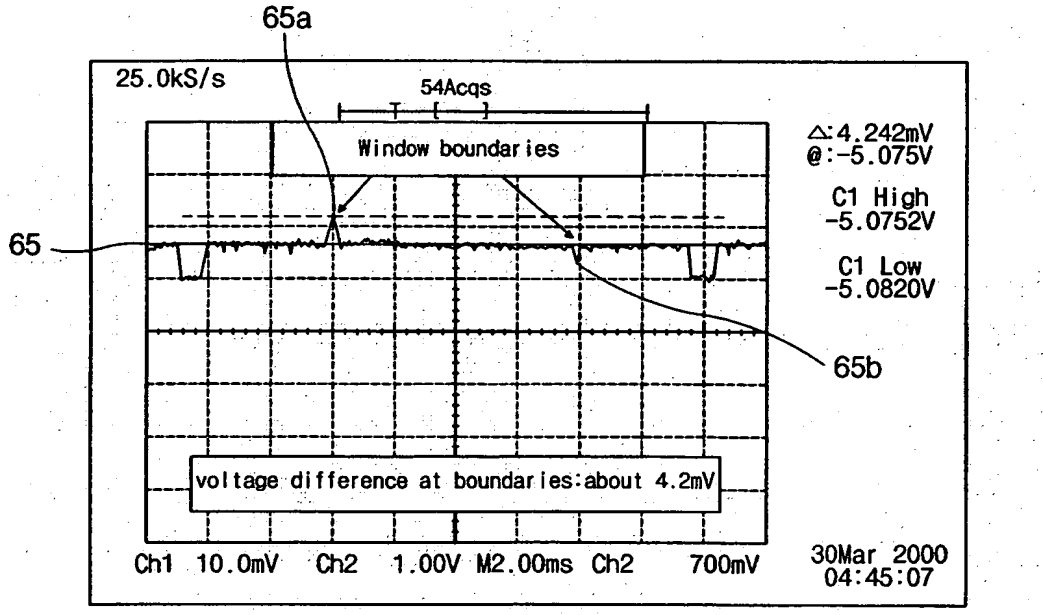
[Fig. 4]



[Fig. 5]


64
t_1
t_2
t_3
63
61

[Fig. 6A]


65a
25.0kS/s
54Acqs
Window boundaries
△:4.242mV
@:-5.075V
C1 High
-5.0752V
C1 Low
-5.0820V
65
65b
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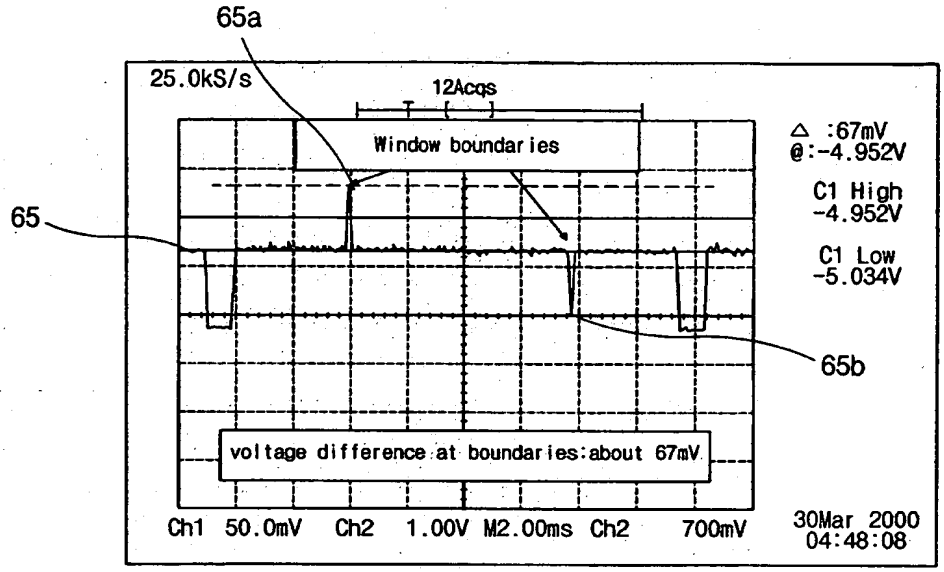
30Mar 2000
04:45:07

[Fig. 6B]


65a
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12Acqs
Window boundaries
65
△ :67mV
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C1 High
-4.952V
C1 Low
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65b
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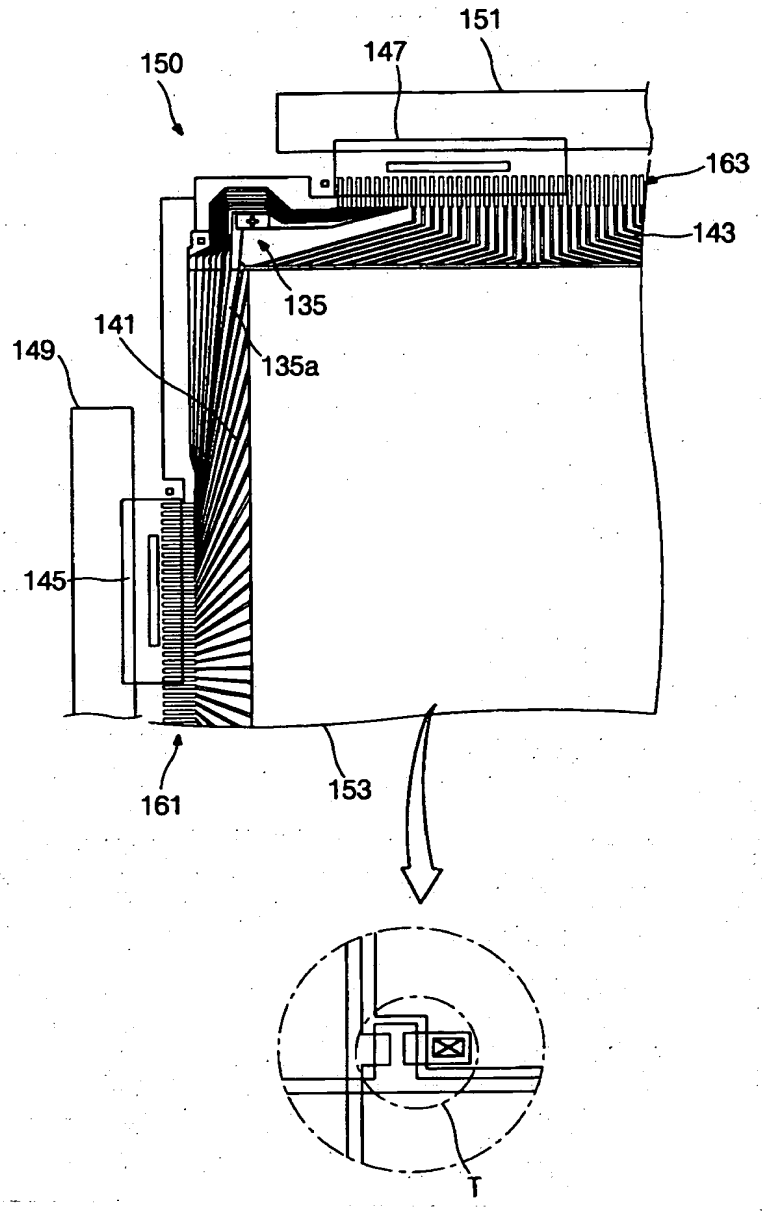
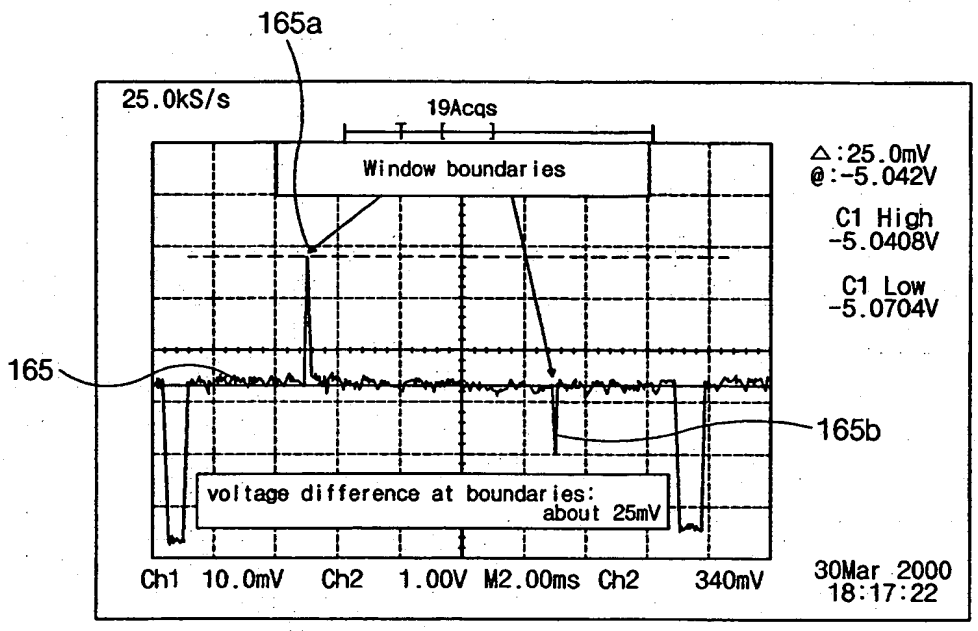
30Mar 2000
04:48:08

[Fig. 7]



[Fig. 8]


165a
25.0kS/s
19Acqs
Window boundaries
△:25.0mV
@:-5.042V
C1 High
-5.0408V
C1 Low
-5.0704V
165
165b
voltage difference at boundaries:
about 25mV
Ch1 10.0mV Ch2 1.00V M2.00ms Ch2 340mV
30Mar 2000
18:17:22